IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2023

CIRCUITS AND SYSTEMS

Wednesday 17 May 14:30

Time allowed: 2 hours

There are THREE questions on this paper.

Answer ALL questions.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : P.Y.K. Cheung
Second Marker(s) : A. Zhao

Information for Candidates:

The following notation is used in this paper:

1. Unless explicitly indicated otherwise, digital circuits are drawn with their inputs on the left and their outputs on the right.
2. Within a circuit, signals with the same name are connected together even if no connection is shown explicitly.
3. The notation X[2:0] denotes the three-bit number X2, X1 and X0. The least significant bit of a binary number is always designated bit 0.

1. (a) Given that $1 + x^2 + x^3 + x^4 + x^8$ is a primitive polynomial, design in SystemVerilog an 8-bit pseudo-random binary sequence generator module with the interface defined in *Figure 1.1*.

[6]

Assuming the sequence starts with the value 8'h02, write down the first 5 values of the sequence.

[4]

```
module pseudo8 (
    input logic         rst,    // reset to initial state
    input logic         clk,    // clock input
    output logic [7:0]  random  // 8-bit pseudo random number
);
```

Figure 1.1

(b) An 8-bit microprocessor system with an address bus *addr[15:0]* and a data bus *data[7:0]* contains an address decoder module that produces three chip select signals: CS_FLASH, CS_RAM, and CS_IO. The Boolean equations for these three signals are:

$$CS\_FLASH = \overline{A15} \,\&\, \overline{A14} \,\&\, \overline{A13}$$
$$CS\_RAM \quad = \overline{A15} \,\&\, A14$$
$$CS\_IO\_CS \quad = A15 \,\&\overline{A14} \,\&\, \overline{A13} \,\&\, A12 \,\&\, A11 \,\&\, \overline{A10}$$

(i) Determine the address range and number of locations associated with each chip select signal.

[6]

(ii) Implement the decoder circuit in SystemVerilog with the module interface defined in *Figure 1.2*.

[2]

(iii) The only RAM chips available are asynchronous 8k x 8bit RAM devices with address signals *A [12:0]* and data signals *D[7:0]*. Draw a schematic diagram showing how the microprocessor may be interfaced to one or more RAM chips to implement the random-access memory for this microprocessor system for the given address range for RAM.

[4]

```
module decoder (
    input  logic [15:0]  addr,      // address bus
    output logic         CS_FLASH,  // chip-select signal for flash memory
    output logic         CS_RAM,    // chip-select signal for RAM
    output logic         CS_IO      // chip-select signal for input-output
);
```

Figure 1.2

(c) *Figure 1.3* shows a pipelined circuit with three flip-flops: FF1, FF2 and FF3, and two combinational logic circuit modules: P and Q. FF1 and FF3 are rising-edge triggered while FF2 is falling-edge triggered. For all flip-flops, the clock-to-output delay is 1 ns and the setup time is 2 ns. The propagation delays of P and Q are in the range of 3 ns – 5 ns and 4 ns – 8 ns respectively. You may assume that the hold times of all flip-flops are zero.

(i) If the clock signal is symmetrical and has a mark-space ratio of 1:1, derive the maximum operating frequency of the circuit.

[5]

(ii) If the clock signal is non-symmetrical, what is the maximum operating frequency of the circuit and with what mark-space ratio?

[3]

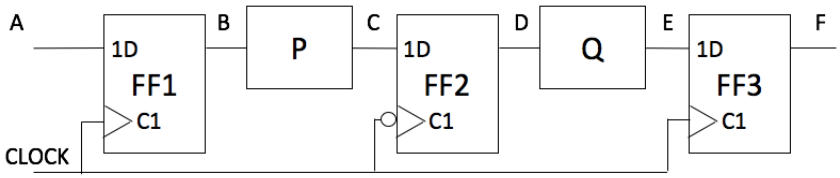


Figure 1.3

(d) *Figure 1.4* shows the circuit of a finite state machine FSM with four internal states and an output signal *OUT*. The register is clocked by the signal *CLOCK* and synchronously reset to zero by the signal *RST*. The logic block is defined by the following Boolean equations with *S1* and *S0* being the current state variables and *IN* is the input signal:

$$NS1 = (IN + \overline{S1}) \cdot S0 + \overline{IN} \cdot S1 \cdot \overline{S0}$$
$$NS0 = IN \cdot \overline{S1} + \overline{IN} \cdot \overline{S0}$$
$$OUT = \overline{S1} \cdot \overline{S0} + S1 \cdot S0$$

(i) Draw the state diagram of the FSM.

[4]

(ii) Based on the state diagram, design in SystemVerilog the module FSM using the interface signal shown in *Figure 1.4*.

[4]

(iii) The FSM is implemented on an Intel MAX10 FPGA which consists of arrays of logic elements (LEs), each containing a register and a 4-input Look Up Table. State with justifications the minimum number of logic elements required to implement this FSM.

[2]

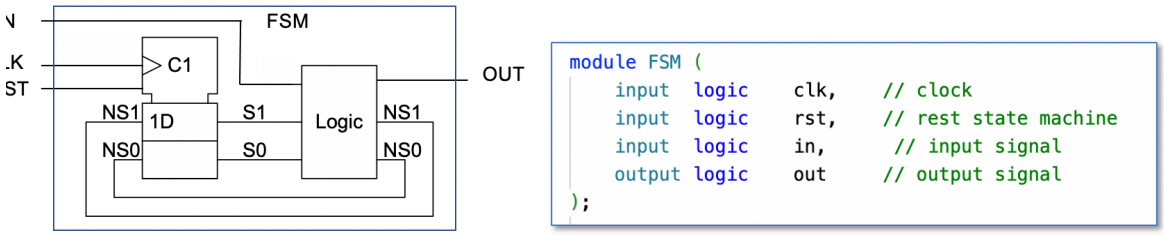


Figure 1.4

(e) *Figure 1.5* shows an inverting amplifier circuit constructed from an operational amplifier that has a single power supply at 5V and with a gain-bandwidth product of 1MHz, two resistors R1 and R2, and a voltage source at 2.5V.

(i) Write down an equation for the gain of this amplifier.

[2]

(ii) Given that the amplifier has a gain of -14 and R1 = 2.2kΩ, determine the value of R2.

[2]

(iii) A design is required to provide an overall gain of -200 for a signal with frequency component from 1kHz to 50kHz. Explain why the circuit in *Figure 1.5* is unable to achieve the specification.

[2]

(iv) Hence or otherwise, design an additional circuit using a second operational amplifier to meet the required specification.

[4]

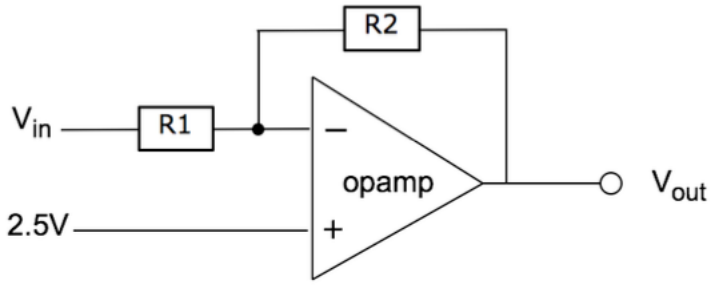


Figure 1.5

2. The Appendix shows part of the datasheet for an LM397 analogue comparator. The same datasheet is also provided as a separate document for your convenience.

a) Briefly explain the significance of the following electrical characteristics from the datasheet with respect to the performance of the comparator:

(i) Input offset voltage V_{OS}
(ii) Output sink current I_O
(iii) Voltage Gain A_V
(iv) Propagation Delay (High to Low) t_{pHL}

[8]

b) *Figure 2.1* shows the LM397 comparator being driven by an input voltage V_{IN}, where

$$V_{in} = 2\sin(2\pi \times 5 \times 10^5 t) + 2.5\ V.$$

Sketch the output waveform V_{OUT} for $0 \leq t \leq 4\mu s$, showing the time at which the output changes states. You may assume that the output of the comparator is driving a load resistance of 5.1kΩ and a load capacitance of 15pF, and you may use the typical values specified in the datasheet. State any other relevant assumptions.

[7]

c) What is "hysteresis" in the context of an analogue comparator circuit and why may it be useful?

[4]

d) *Figure 2.2* shows a LM397 configure with hysteresis. What are the switching threshold voltages for this comparator circuit?

[6]

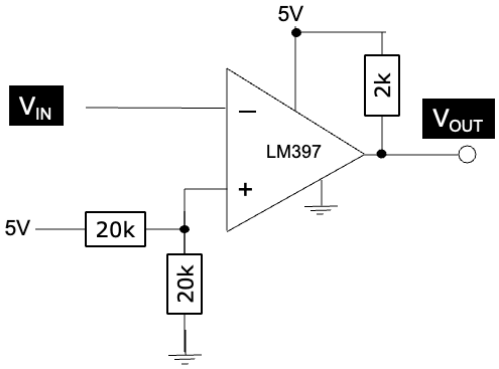


Figure 2.1

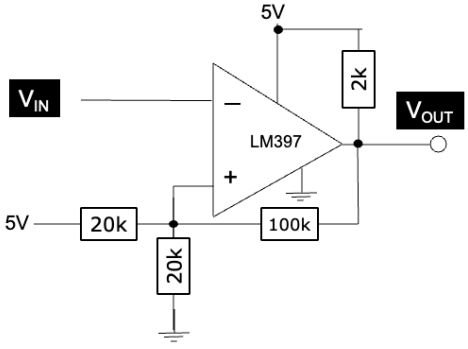


Figure 2.2

3. *Figure 3.1* shows an analogue-to-digital converter (ADC) design using the dual-slope technique. The converter consists of an op-amp A1 configured as an integrator with an output signal *X*, an analogue comparator A2 that produces a digital compatible output *Y*, two 2-pole electronic switches S0 and S1, and a digital controller M1. Both A1 and A2 operate with a ±15V power supply.

   The ADC works according to the timing diagram shown in *Figure 3.2.* When the ADC is in idle state, C0 is low causing the switch S0 to short circuiting the capacitor C. At time t_0 a conversion is initiated with a positive edge on the *start* signal. The input signal *Vin* is applied to the integrator via the switch S1. After integrating the input voltage *Vin* for 20ms, S1 switches the integrator input a -10V reference voltage at time t_1 so that the capacitor C is discharged at a constant current until the voltage at the output of the integrator reaches 0V at time t_2. The converter 12-bit data is then sent to the output *data[11:0]*, and the *done* output signal is asserted to indicate that the data is valid.

   a) Explain why the duration $k = t_2 - t_1$ is proportional to the input voltage *Vin*. Derive an equation that relates the duration *k* to *Vin*.

   [6]

   b) What is the voltage range of *Vin* within which the ADC can operate?

   [2]

   c) What is the maximum sampling rate that this ADC can operate and why?

   [2]

   d) Assume that C = 1uF, what value of R would you choose and why?

   [2]

   e) *Figure 3.3* shows the design of the controller M1. It consists of three counters: CTR1, CTR2 and CTR3, and finite state machine FSM. Assuming that CLK is a symmetrical clock signal at 50MHz, design the digital controller M1 that performs ADC conversion as one or more SystemVerilog modules.

   [13]

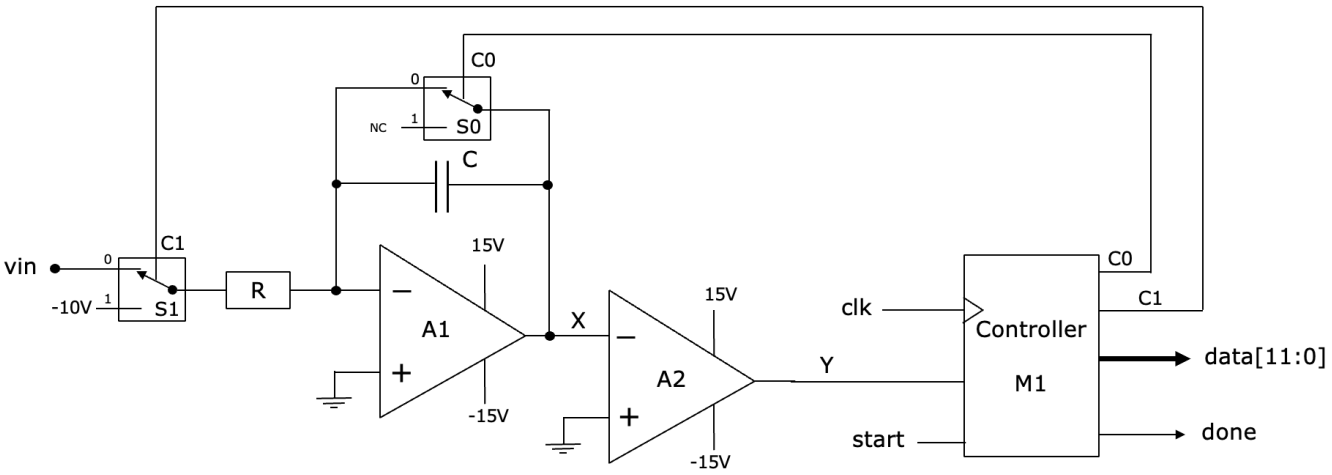


Figure 3.1

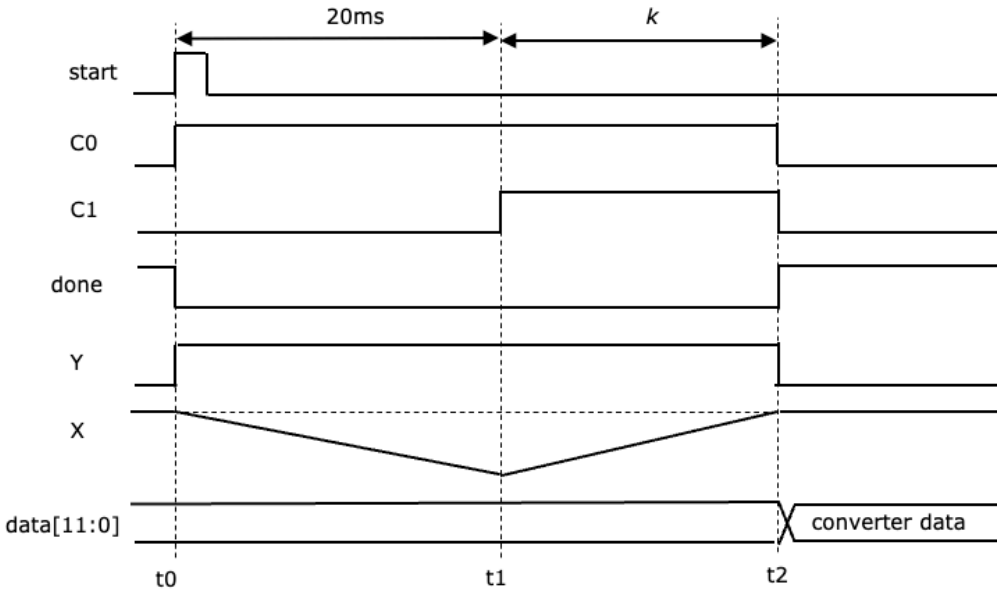


Figure 3.2

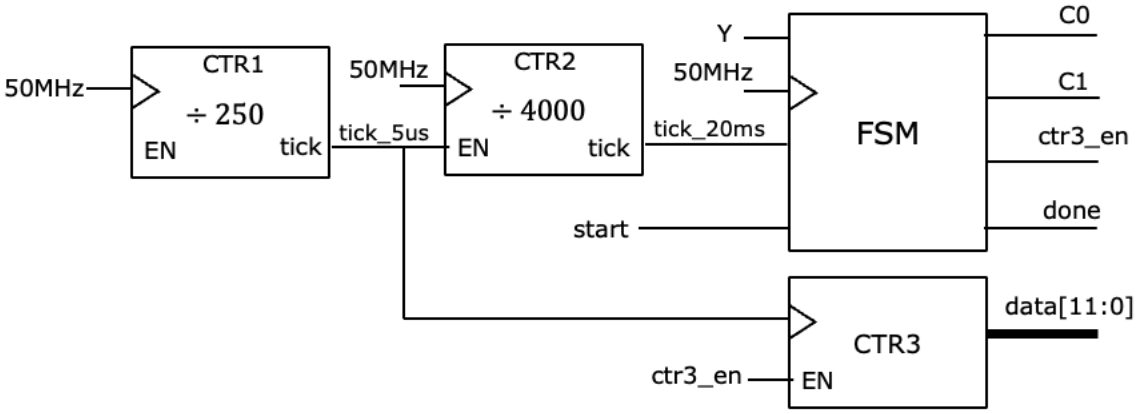


Figure 3.3

National Semiconductor

June 2001

LM397
Single General Purpose Voltage Comparator

General Description

The LM397 is a single voltage comparator with an input common mode that includes ground. The LM397 is designed to operate from a single 5V to 30V power supply or a split power supply. Its low supply current is virtually independent of the magnitude of the supply voltage.

The LM397 features an open collector output stage. This allows the connection of an external resistor at the output. The output can directly interface with TTL, CMOS and other logic levels, by tying the resistor to different voltage levels (level translator).

The LM397 is available in space saving SOT23-5 package and pin compatible to TI's TL331, single differential comparator.

Features

(T_A = 25˚C. Typical values unless otherwise specified).

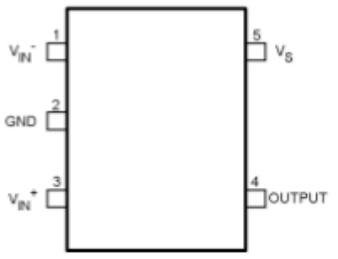
- SOT23-5 package
- Industrial operating range –40˚C to +85˚C
- Single or dual power supplies
- Wide supply voltage range 5V to 30V
- Low supply current 300μA
- Low input bias current 7nA
- Low input offset current ±1nA
- Low input offset voltage ±2mV
- Response time 440ns (50mV overdrive)
- Input common mode voltage 0 to V_S - 1.5V

Applications

- A/D converters
- Pulse, square wave generators
- Peak detector
- Industrial applications

Connection Diagram

SOT23-5



Top View

Typical Circuit

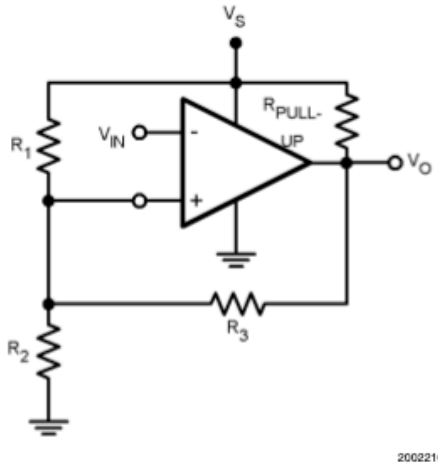


FIGURE 1. Inverting Comparator with Hysteresis

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
5-Pin SOT-23	LM397MF	C397	1k Units Tape and Reel	MF05A
	LM397MFX		3k Units Tape and Reel	

 DS200221 www.national.com

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	
Human Body Model	2KV (Note 2)
Machine Model	200V (Note 3)
V_{IN} Differential	30V
Supply Voltages	30V or ±15V
Voltage at Input Pins	−0.3V to 30V
Storage Temperature Range	−65˚C to +150˚C
Junction Temperature (Note 4)	+150˚C
Soldering Information	
Infrared or Convection (20 sec.)	235˚C
Wave Soldering (10 sec.)	260˚C

Operating Ratings (Note 1)

Supply Voltage, V_S	5V to 30V
Junction Temperature Range (Note 4)	−40˚C to +85˚C
Package Thermal Resistance (Note 4)	
SOT23-5	168˚C/W

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25˚C, V_S = 5V. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage	V_S = 5V to 30V, V_O = 1.4V, V_{CM} = 0V		2	7 **10**	mV
I_{OS}	Input Offset Current	V_O = 1.4V, V_{CM} = 0V		1.6	50 **250**	nA
I_B	Input Bias Current	V_O = 1.4V, V_{CM} = 0V		10	250 **400**	nA
I_S	Supply Current	R_L = Open, V_S = 5V		0.25	0.7	mA
		R_L = Open, V_S = 30V		0.30	2	
I_O	Output Sink Current	V_{IN^+} = 1V, V_{IN^-} = 0V, V_O = 1.5V	6	13		mA
$I_{LEAKAGE}$	Output Leakage Current	V_{IN^+} = 1V, V_{IN^-} = 0V, V_O = 5V		0.1		nA
		V_{IN^+} = 1V, V_{IN^-} = 0V, V_O = 30V		1		μA
V_{OL}	Output Voltage Low	I_O = −4mA, V_{IN^+} = 0V, V_{IN^-} = 1V		180	400 **700**	mV
V_{CM}	Common-Mode Input Voltage Range	V_S = 5V to 30V (Note 7)	V_S - 1.5V **V_S - 2V**		0 **0**	V

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25˚C, V_S = 5V. **Boldface** limits apply at temperature extremes. (Continued)

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
A_V	Voltage Gain	V_S = 15V, V_O = 1.4V to 11.4V, R_L > = 15kΩ connected to V_S		120		V/mV
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 5mV, R_L = 5.1kΩ connected to 5V, C_L = 15pF		900		ns
		Input Overdrive = 50mV, R_L = 5.1kΩ connected to 5V, C_L = 15pF		250		
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 5mV, R_L = 5.1kΩ connected to 5V, C_L = 15pF		940		ns
		Input Overdrive = 50mV, R_L = 5.1kΩ connected to 5V, C_L = 15pF		440		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF.

Note 3: Machine model, 0Ω in series with 200pF.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: The input common-mode voltage of either input should not be permitted to go below the negative rail by more than 0.3V. The upper end of the common-mode voltage range is V_S - 1.5V at 25˚C.

